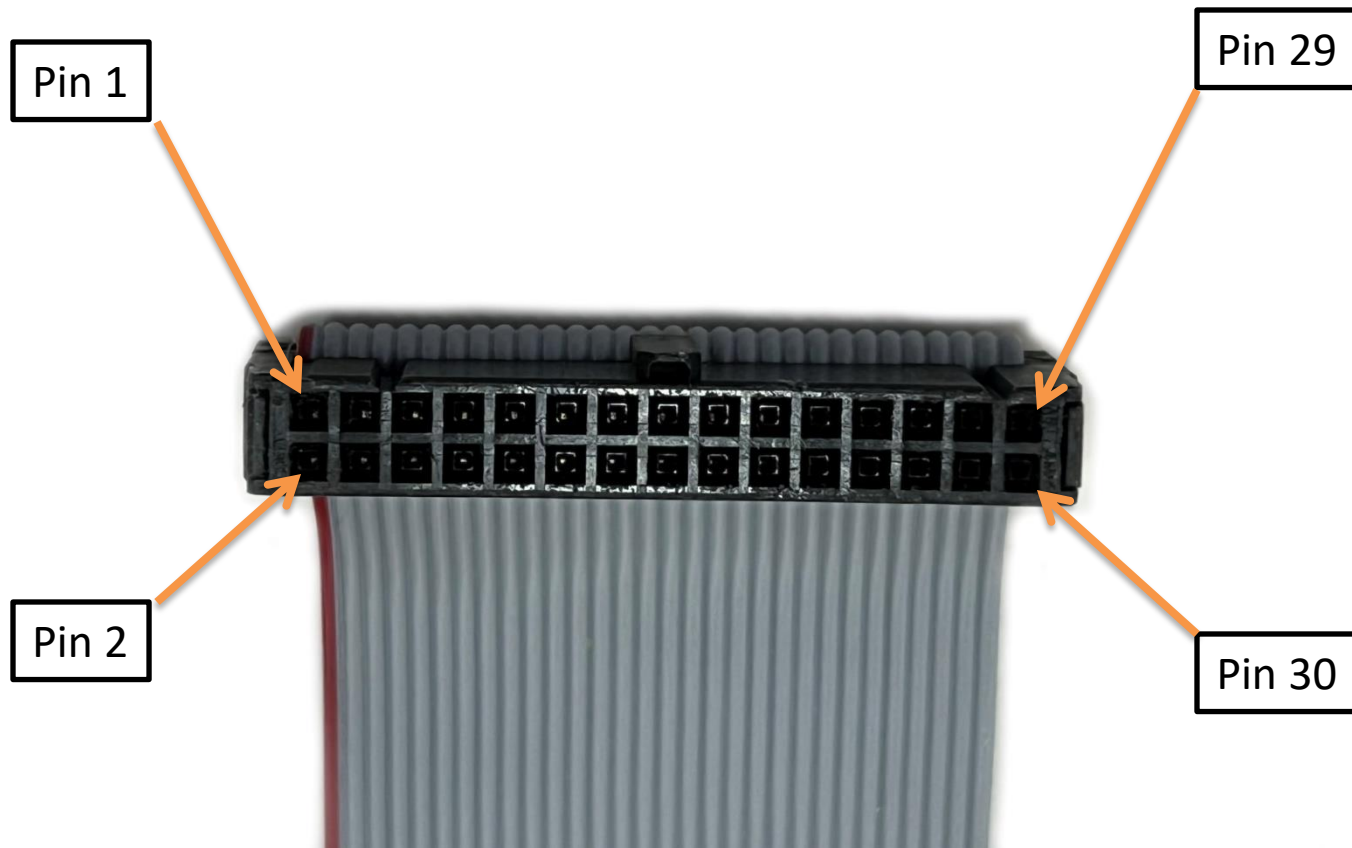


LCC Array Integrated Cable Pinout Description

Purpose and Scope

- This document is intended to give a pin by pin description and overview for the Cabled LCC version of the Infrared Materials Multiplexer
- For more detailed information regarding operation of the muxiplexer and its digital interface please see the companion document AM256.

LCC Array IDC Connector



Cable Pinout Table

Pin #	Signal Name	Signal Type	Notes:
1,2	TEC+	TE Drive	Drive within TE cooler specifications
3,4	TEC-	TE Drive	Drive within TE cooler specifications
5	NC	NC	Make no connection
6	INT_CLK	Digital	TTL - control over shoot and undershoot to < 300mV
7	SERIAL_DATA	Digital	TTL - control over shoot and undershoot to < 300mV
8	SERIAL_CLK	Digital	TTL - control over shoot and undershoot to < 300mV
9	CFG_LOAD_CLK	Digital	TTL - control over shoot and undershoot to < 300mV
10	START_FRAME	Digital	TTL - control over shoot and undershoot to < 300mV
11	DAC_LD_CLK	Digital	TTL - control over shoot and undershoot to < 300mV
12,23,24	VDD	Mux Power	5VDC +/- 250 mV
13	PIXEL_CLK	Digital	TTL - control over shoot and undershoot to < 300mV
14,15,21,25,27	VSS (GND)	Ground	
16	DAC_VH	Analog Ref	Adjustable analog voltages 0.7V to 2.5V, low noise, source impedance <= 10 ohms
17	DAC_VL	Analog Ref	
18	NC	NC	Make no connection
19,29	Therm 1A	TE Sense	Thermistor connections - 4 wire Kelvin connection
20,30	Therm 1B	TE Sense	
22	GSKIM	Analog Ref	Adjustable analog voltage 0.4V to 2.5V, low noise
26	BUFOUT	Analog Output	Analog Mux output from LT6220 buffer - 39 ohm output impedance
28	DETBias	Analog Ref	Very low noise analog voltage, adjustable from VMUX to 12 Volts.

Signal Notes: TEC(+/-)

- Pins 1 & 2 (TEC+) and 3 & 4 (TEC-) connect directly to the two sides of the thermoelectric cooler element.
 - The signals are doubled up to provide increased current capacity
 - A cooler controller with smooth, DC like, outputs is best. A switching controller with high current pulses on these lines could adversely effect the performance of the array.

Signal Notes: TE Sense

- Pins 19 and 20, and pins 29 and 30 are connected to the thermistor inside the LCC package.
 - The two pairs of lines separate at the PCB pad for the thermistors.
 - One pair of connections is for carrying current from the controller's bridge circuit, the other two are a voltage sense point (kelvin connection). It is up to the user to make use of this if they wish.

Signal Notes: VDD (Mux Power)

- The mux power, VDD, comes in on three pins: 12, 23, and 24.
- It is recommended to connect to all three pins.
- Mux power, VDD, should be 5V +/- 250mV. It should be stable and as low noise as practical.
 - The current version of the IMI controller board uses a heavily filtered (5Kohm, 10uF) version of the 5 V supply buffered through a low noise amp (AD8614) that is stable with high capacitance loads

Signal Notes: VSS (Ground)

- The ground, comes in on five pins: 14,15,21,25, and 27. It is recommended to connect ground to all 5 lines.
 - All the ground lines are placed in the ribbon cable to provide EM shielding and separation between different types of signals.
- Avoid dumping any switching currents into the LCC package grounds. Ground is the backside of the IC die and noise on ground can degrade the IC operation and noise performance.

Signal Notes: DETBIAS

- The DETBIAS, Pin 12, (aka Detector Bias, Detector Common) is the DC bias voltage applied to one side of the photo conductive detector.
 - Each pixel in the mux operates as its own CTIA, taking in detector current and integrating it to produce a voltage output.
 - The detector bias provides the current to integrate
 - Any noise on DETBIAS will get amplified with the signal, the two are indistinguishable to the multiplexer
 - Be mindful of source impedance. A 10Mohm nominal detector impedance is only about 40Kohms when there are 256 of them in parallel. The source impedance for the DETBIAS should be low.
 - Noise issues on DETBIAS will generally present as identical movement of all pixels in the array. (temperature stability issues presents in the same way, but usually at a lower frequency)
- Since one side of the detector is connected to an internal multiplexer node it is not possible to know the exact voltage across any give detector.
 - Simulations put the internal node at around 0.5 volts below VDD.
 - The Infrared materials supplied drive electronics can produce DETBIAS voltages from 0.5V to 7V (12V referenced to ground). This is a useful range in most cases. Very high detector impedances may be able to benefit from even higher DETBIAS voltages.
- There are three primary sources of noise in the system, DETBIAS noise, electronics noise (from the mux) and detector noise.
 - As the magnitude of DETBIAS is increased the signal increases, but so does the noise.
 - Once DETBIAS is high enough that detector noise is above electronics noise then any further increase in DETBIAS will not improve SNR
 - Not all cases can reach detector noise limited performance, it depends on many variables.

Signal Notes: BUFOUT

- The BUFOUT pin is the analog output (pixel stream) and is located on pin 26 of the cable.
- The output is from the mux, but buffered through a RRIO unity gain buffer opamp (LT6220)
 - There is also a series 39ohm resistor in the output path.
 - This resistor forms part of the band limiting filter at the input to the A/D converter. It also damps the over/under shoot on pixel edges.
- The BUFOUT has a voltage limited range of approx 0.2V to 4.8V. The actual usable range from the mux is closer to 0.5V to 4.5V

Signal Notes: DAC_VH & VL

- DAC_VH, Pin 16, and DAC_VL, Pin 17, are precision analog voltages used to set the operating limits of the per pixel current skim. It is the per pixel current skim that allows the pixel to pixel non uniformity to be reduced, usually by more than 100 : 1
- These voltages need to be low noise, low output impedance, precise (10 bit resolution or better), and stable voltages.
 - Recommended output impedance is ≤ 10 ohms.
 - Recommended range is 0.7V to 2.5V
- The DAC_Vx voltages set the upper and lower limit on an internal set of 256 DACs inside the mux that control the subtraction current source in each pixel.
- The voltages do not act linearly, the MOSFET gate has a square law relationship between the voltage applied and the current subtracted.
 - Each pixel has its own subtraction FET with different threshold and gain characteristics.
 - These factors make computing the voltage required to work with an array impossible. The optimal solution must be arrived at by an iterative process.
 - Typically the Pixel DAC skim can remove dark currents in the 0 to 1uA range.

Signal Notes: GSKIM

- GSKIM, Pin 22, is precision analog voltages used to operate a global dark current skim circuit
 - Each pixel has a global skim FET that skims the dark current from the detector.
 - The gates of all 256 global skim FETs are tied together and connected to the GSKIM pad.
- GSKIM need to be low noise, precise (10 bit resolution or better), and stable voltage.
 - Since the GSKIM is connected only to FET gates it has a very high load impedance ($> \text{Gigaohms}$)
 - Recommended range is 0.4V to 2.5V (note at 0.4V the GSKIM current subtraction FET will be completely off)
- The voltage do not act linearly, the MOSFET gate has a square law relationship between the voltage applied and the current subtracted.
 - Each pixel has its own subtraction FET with different threshold and gain characteristics.
 - These factors make computing the voltage required to work with an array impossible. Typically the Gskim FET can remove dark currents in the 0 to 10uA range.
 - The smaller physical size of the Gskim FET makes it noisier than the per pixel skim DAC FET. For that reason we recommend that the global skim only be used on arrays that require large ($>1\mu\text{A}$) of dark current skim.

Signal Notes: {All Digital Signals}

- All digital signals accept standard TTL signal levels.
- All digital signals have an internal pullup on the IC. This is approximately a 4uA pull up.
- Avoid overshoot and undershoot on the digital lines. Any excursion more than 300mV may drive current directly into the die, disrupting the operation.

Signal Notes: INT_CLK

- INT_CLK, Pin 6, is the Integration Clock
- INT_CLK controls when the mux charge well accumulates charge and when it is in reset.
 - In general, when it is low the charge wells are all in reset, when it is high the charge wells are integrating detector current.
- The positive (high) width of INT_CLK is almost the same as the integration time
 - There is an asynchronous timing generation circuit that operates off the rising and falling edges of INT_CLK to perform needed internal processes.
 - An Async timing generator is used so that all clocking can be halted during integration.
 - The timing generator sets a lower limit on integration, which we have set (conservatively) at 10us.
 - The upper integration time limit is generally set by the detector uniformity / detector bias / charge well size combination
- See the AM256 document for further details on integration timing

Signal Notes: PIXEL_CLK

- PIXEL_CLK, Pin 13, is the Pixel Clock, or readout clock.
- PIXEL_CLK controls the readout of the linear mux array.
 - Dual edged so that there is no clock transition during the pixel settling time
 - The readout is reversible, and has settable start and stop points for windowing
- The maximum readout speed is 4 mega pixels per second, which equates to a 2MHz pixel clock frequency (because it is a dual edge clock)
 - Min readout speed is a wide target, with leakage induced droop being the biggest factor in slow readouts. A recommended guideline is that the entire readout should be completed within 10ms, which equates to a min readout speed of approx 25Kpixels per second (12.5KHz PIXEL_CLK speed)
- Pixel readout is initiated by the interaction of START_FRAME (pin 10) and PIXEL_CLK
- See the AM256 document for further details on readout timing

Signal Notes: START_FRAME

- START_FRAME, Pin 10, is the start frame signal that initiates a pixel readout.
- START_FRAME initiates the readout of the linear mux array
 - Dual edged so that there is no clock transition during the pixel settling time
 - The readout is reversible, and has settable start and stop points for windowing
- The maximum readout speed is 4 mega pixels per second, which equates to a 2MHz pixel clock frequency (because it is a dual edge clock)
 - Min readout speed is a wide target, with leakage induced droop being the biggest factor in slow readouts. A guideline is that the entire readout should be completed within 10ms, which equates to a min readout speed of approx 25Kpixels per second (12.5KHz PIXEL_CLK speed)
- Pixel readout is initiated by the interaction of START_FRAME (pin 10) and PIXEL_CLK
 - FRAME_START is clocked in on an edge of PIXEL_CLK (which is a dual edge clock)
 - On the very next edge of PIXEL_CLK the first pixel will come out and begin settling on the output of the multiplexer
- See the AM256 document for further details on readout timing

Signal Notes: SERIAL_CLK

- SERIAL_CLK, Pin 8, is the serial clock for both the serial control register and the loading of the per pixel subtraction coefficients.
 - Rising edge clock
 - Together with SERIAL_DATA, CFG_LD_CLK, and DAC_LD_CLK they form the serial interface to the multiplexer
 - A 50% duty cycle is recommended with a maximum clock rate of 10MHz.
- The Serial Control Register must be loaded each time the mux is powered up or it will not operate as expected. See AM256 doc for more information on the serial control register.
- See the AM256 document for further details on the serial interface

Signal Notes: SERIAL_DATA

- SERIAL_DATA, Pin 7, is the serial data input for both the serial control register and the loading of the per pixel subtraction coefficients.
 - The data line is clocked in on the rising edge clock or SERIAL_CLK
 - Together with SERIAL_CLK, CFG_LD_CLK, and DAC_LD_CLK they form the serial interface to the multiplexer
 - A 10ns setup and hold time prior to the edge of SERIAL_CLK is recommended
- The Serial Control Register must be loaded each time the mux is powered up or it will not operate as expected. See AM256 doc for more information on the serial control register.
- See the AM256 document for further details on the serial interface

Signal Notes: CFG_LOAD_CLK

- CFG_LOAD_CLK, Pin 9, is the loading (latching) clock for the mux serial configuration register.
 - On the rising edge of CFG_LOAD_CLK the data present in the serial configuration register is latched into the multiplexer.
 - Together with SERIAL_CLK, SERIAL_DATA, and DAC_LD_CLK they form the serial interface to the multiplexer
 - It is recommended that the rising edge of CFG_LOAD_CLK occur at least 10ns after the rising edge of SERIAL_CLK that is loading the serial configuration register.
- The Serial Control Register must be loaded each time the mux is powered up or it will not operate as expected. See AM256 doc for more information on the serial control register.
- See the AM256 document for further details on the serial interface

Signal Notes: DAC_LD_CLK

- DAC_LD_CLK, Pin 11, is the loading (latching) clock for the 8 bit per pixel current subtraction DAC.
 - The per pixel DAC registers can only be updated during a multiplexer readout cycle. The DAC loading system uses the readout to point to the pixel that is to have its DAC updated.
 - Once the readout is pointing at a pixel the last 8 bits loaded into the serial interface can be latched into the pixel DAC on the rising edge of DAC_LD_CLK.
 - It is recommended that the rising edge of CFG_LOAD_CLK occur at least 10ns after the rising edge of SERIAL_CLK that is loading the serial interface.
- The per pixel DAC registers power up in random values.
- See the AM256 document for further details on the serial interface and pixel DAC loading