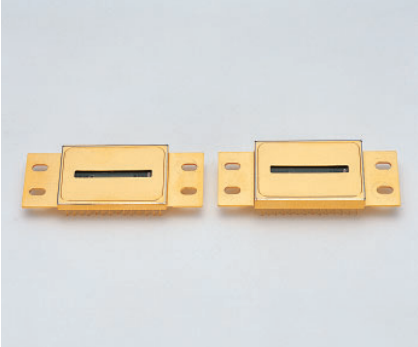
HAMAMATSU

InGaAs linear image sensors



G9201 to G9204 series

Image sensor for DWDM wavelength monitor

The G9201 to G9204 series are InGaAs linear image sensors designed for WDM monitor detectors in optical communications. These linear image sensors contain a CMOS charge amplifier array, a CDS circuit, an offset compensation circuit, a shift register and a timing generator, along with an InGaAs photodiode array, and deliver high sensitivity and stable operation in the near infrared range. The package is hermetically sealed for high reliability and the light input window has an anti-reflective coating to improve the light detection efficiency.
The signal processing circuit on the CMOS chip allows selecting two conversion efficiencies (CE) by external voltage. A wide dynamic range can be obtained when the image sensor is operated at CE=16 nV/e^-, while a high gain can be obtained at CE=320 nV/e^-.

Features

- **Wide dynamic range**
- **Low noise and low dark current**
- **Two selectable conversion efficiencies**
- **Anti-saturation circuit**
- **CDS circuit *1**
- **Offset compensation circuit**
- **Simple operation (by built-in timing generator *2)**
- **High resolution: 25 µm pitch (512 ch)**
- **Low crosstalk**
- **256 ch: 1 video line**
  512 ch: 2 video lines

Applications

- **DWDM wavelength monitor**
- **Optical spectrum analyzer**

Accessories (Optional)

- **InGaAs multichannel detector head C8061-01 *3**
- **Multichannel detector head controller C7557-01 *3**

Selection guide

Type No.	Cooling	Number of pixels	Pixel pitch (µm)	Pixel size [µm (H) × µm (V)]	Spectral response range (µm)	Defective pixel
G9201-256S	One-stage TE-cooled	256	50	50 × 250	0.9 to 1.67 (-10 °C)	0
G9202-512S	One-stage TE-cooled	512	25	25 × 250	0.9 to 1.67 (-10 °C)	
G9203-256D *4	Non-cooled	256	50	50 × 500	0.9 to 1.7 (25 °C)	
G9203-256S	One-stage TE-cooled				0.9 to 1.67 (-10 °C)	
G9204-512D *4	Non-cooled	512	25	25 × 500	0.9 to 1.7 (25 °C)	
G9204-512S	One-stage TE-cooled				0.9 to 1.67 (-10 °C)	

*1: A major source of noise in charge amplifiers is the reset noise generated when the integration capacitance is reset. A CDS circuit greatly reduces this reset noise by holding the signal immediately after reset to find the noise differential.
*2: In conventional image sensor operation, external PLD (programmable logic device), etc. is used to input the required timing signals. However, the G9201 to G9204 series image sensors internally generate all timing signals on the CMOS chip just by supplying CLK and RESET pulses. This makes it simple to set the timings.
*3: The G9203-256D and G9204-512D are not available for the C7557-01.
*4: For the G9203-256D and G9204-512D specifications, see the separate datasheet available from HAMAMATSU.

Absolute maximum ratings

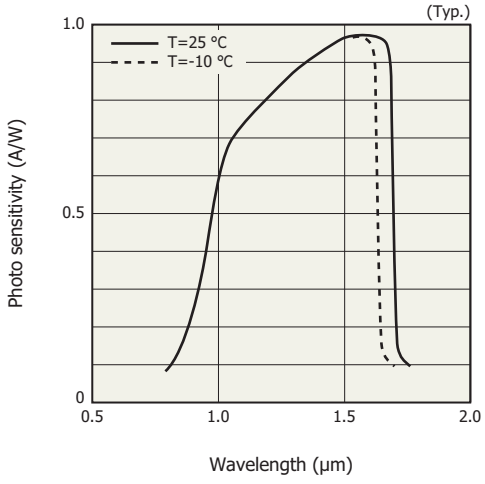
Parameter	Symbol	Value	Unit
Clock pulse voltage	Vϕ	5.5	V
Operating temperature *5	Topr	-40 to +70	°C
Storage temperature *5	Tstg	-40 to +85	°C

*5: No condensation

Electrical characteristics (Ta=25 °C, Vϕ=5 V)

Parameter		Symbol		Min.	Typ.	Max.	Unit
Supply voltage		Vdd		4.9	5.0	5.1	V
		Vref		-	1.26	-	
Supply current		I(Vdd)	256 ch	-	45	50	mA
			512 ch	-	90	100	
		I(Vref)		-	-	1	mA
Ground		Vss		-	0	-	V
Element bias		INP		3.5	4.5	4.6	V
Element bias current		I(INP)		-	-	1	mA
Clock frequency		f		0.1	-	4	MHz
Clock pulse voltage	High	Vϕ		Vϕ - 0.5	Vϕ	Vϕ + 0.5	V
	Low			0	0	0.4	V
Clock pulse rise/fall times		tr ϕ		0	20	100	ns
		tf ϕ					
Clock pulse width		tpw ϕ		100	-	-	ns
Reset pulse voltage	High	V(RES)		Vϕ - 0.5	Vϕ	Vϕ + 0.5	V
	Low			0	0	0.4	V
Reset pulse rise/fall times		tr(RES)		0	20	100	ns
		tf(RES)					
Reset pulse width		tpw(RES)		6000	-	-	ns
Video output voltage	High	V_H		-	4.5	-	V
	Low	V_L		0	1.26	-	
Video data rate		fv		-	f/8	-	Hz

Spectral response



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Electrical and optical characteristics (T=25 °C)

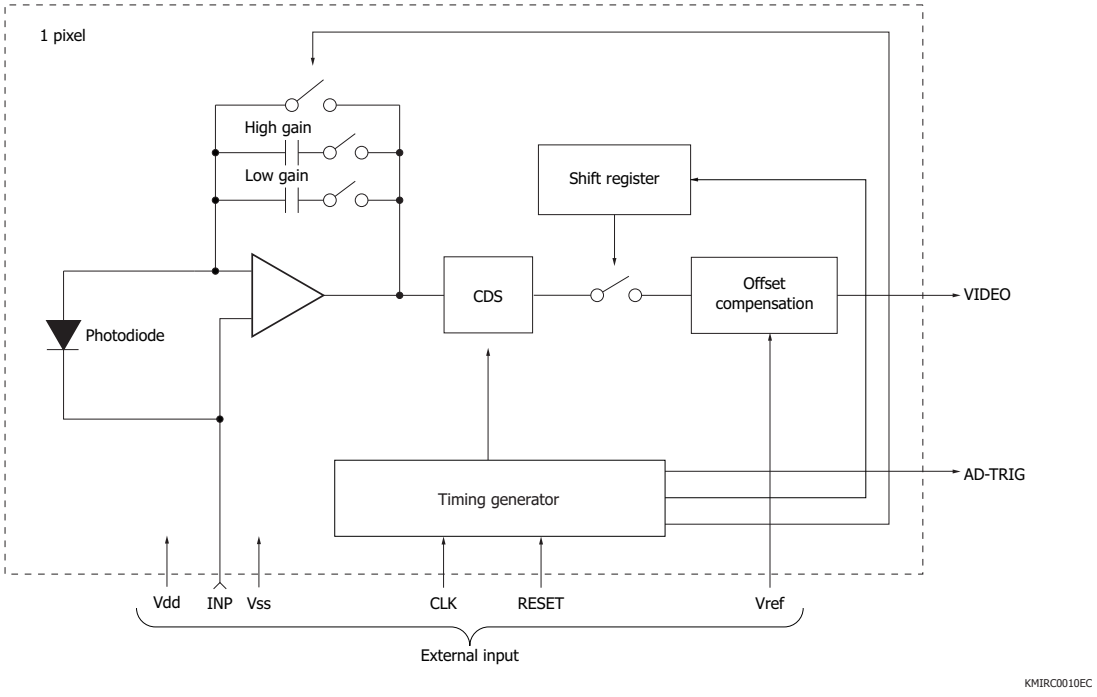
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Peak sensitivity wavelength	λp		-	1.55	-	µm
Saturation charge	Qsat	*6	-	30	-	pC
RMS noise voltage (readout noise)	N	Standard deviation Number of integration=50	-	180	300	µV rms
Photo response non-uniformity	PRNU	*7	-	-	±5	%
Saturation voltage	Vsat		3.0	3.2	-	V

*6: Vϕ=5 V, CE=16 nV/e⁻
*7: 50 % of saturation, integration time=10 ms, after dark output subtraction, excluding first and last pixels.

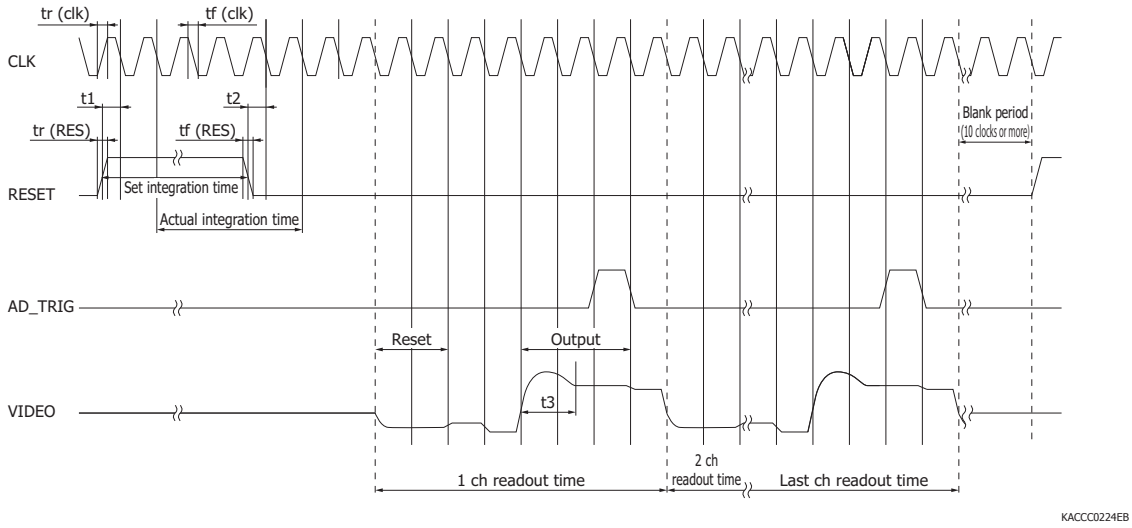
Dark current characteristics (T=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
G9201 series	ID	-	2	10	pA
G9202 series		-	1	5	
G9203 series		-	4	20	
G9204 series		-	1	5	

Equivalent circuit

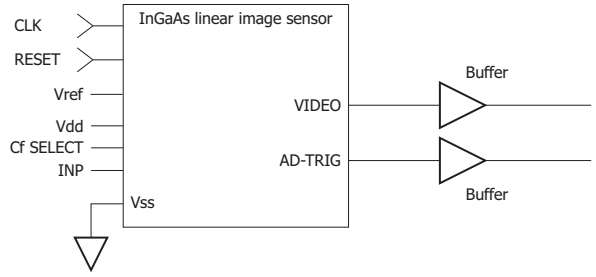


Timing chart

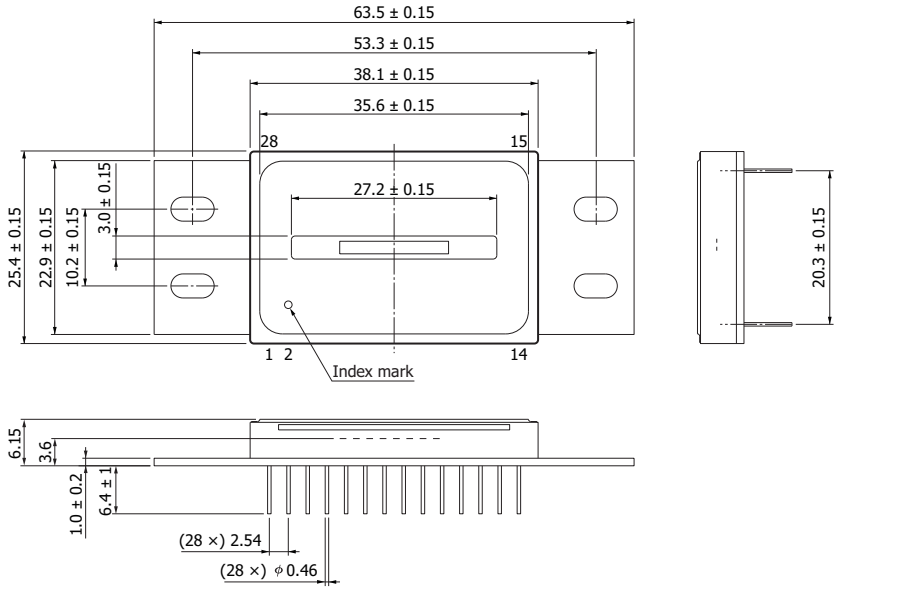


Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	-	0.1	-	4	MHz
Clock pulse width	tpw (clk)	100	-	-	ns
Clock pulse rise/fall times	tr (clk), tf (clk)	0	20	100	ns
Reset pulse width	tpw (RES)	6000	-	-	ns
Reset pulse rise/fall times	tr (RES), tf (RES)	0	20	100	ns
Reset (rise) timing	t1	50	-	-	ns
Reset (fall) timing	t2	50	-	-	ns
Output settling time	t3	-	-	600	ns

Basic circuit connection



Dimensional outline (unit: mm)



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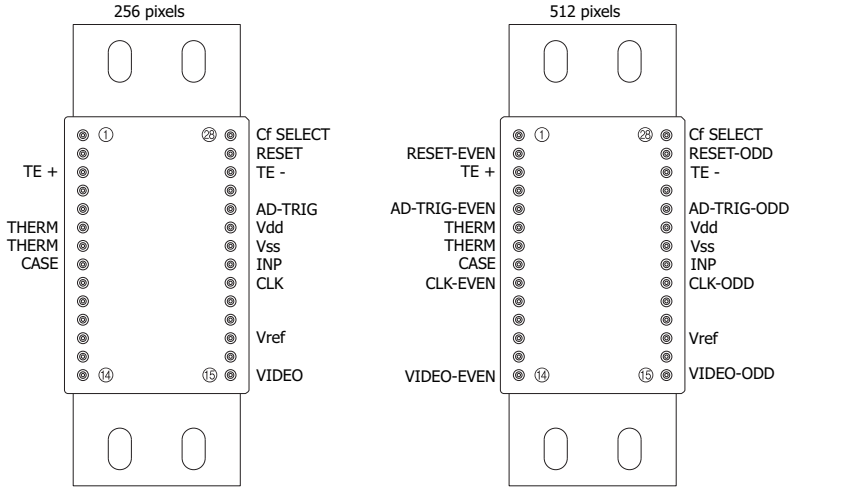
Pin connection (top view)



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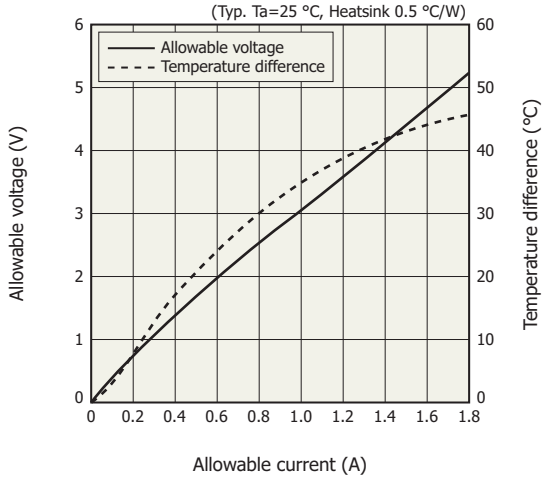
Terminal name	Input/Output	Function and recommended connection
CLK	Input (CMOS logic compatible)	Clock pulse for operating the CMOS shift register
RESET	Input (CMOS logic compatible)	Reset pulse for initializing the feedback capacitance in the charge amplifier formed on the CMOS chip. The width of the reset pulse is integration time.
Vdd	Input	Supply voltage for operating the signal processing circuit on the CMOS chip
Vss	-	Ground for the signal processing circuit on the CMOS chip
INP	Input	Reset voltage for the charge amplifier array on the CMOS chip
Cf SELECT	Input	Voltage that determines the feedback capacitance (Cf) on the CMOS chip. Low gain (CE=16 nV/e^-) at 0 V, and high gain (CE=320 nV/e^-) at 5 V.
CASE	-	This terminal is electrically connected to the package.
THERM	-	Thermistor terminal for monitoring temperature inside the package
TE+, TE-	-	Power supply terminal for the thermoelectric cooler that cools the photodiode array
AD-TRIG	Output	Digital signal for A/D conversion; positive polarity
VIDEO	Output	Analog video signal; positive polarity
Vref	Input	Reset voltage for the offset compensation circuit on the CMOS chip

Specifications of one-stage TE-cooler (Ta=25 °C, Vdd=5 V, INP=4.5 V)

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
TE-cooler allowable current		Ic Max.	-	-	1.8	A
TE-cooler allowable voltage		Vc Max.	-	-	5.0	V
Temperature difference *8	Ic=1.4 A	Δt	40	-	-	°C
Thermistor resistance		Rth	4.85	5.00	5.15	kΩ
Thermistor power dissipation		Pth	-	-	0.2	mW

*8: This is a temperature difference between the surface of active area and the heat radiating portion of package.

One-stage TE-cooler temperature characteristics



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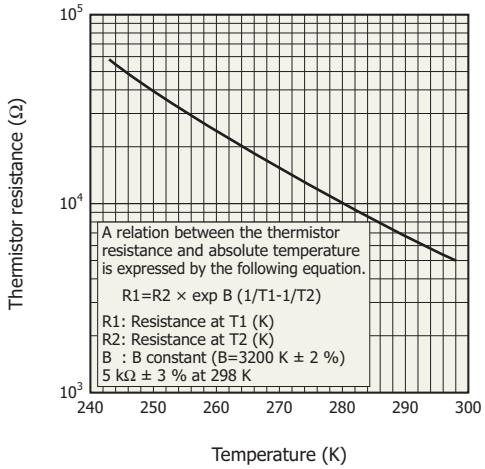
Thermistor temperature characteristic



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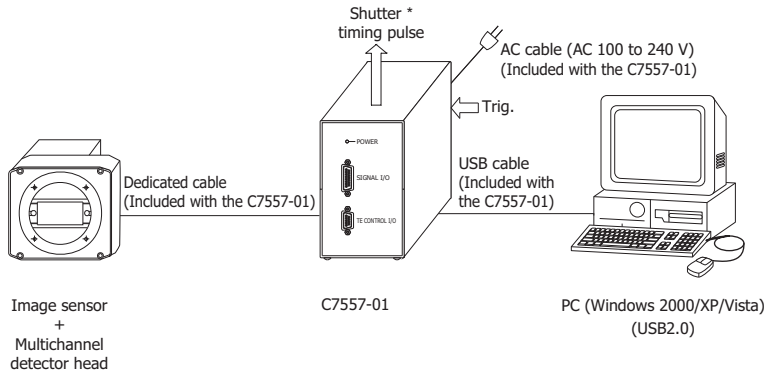
Connection of related products



* Shutter, etc. are not available.

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